AMENDMENTS TO THE CLAIMS

Please amend Claim 3 as indicated below.

Please cancel Claims 1, 2, and 6-8 without prejudice.

A complete listing of all claims is presented below with insertions underlined (e.g., insertion), and deletions struckthrough (e.g., ~~deletion~~):

1. (Cancelled)

2. (Cancelled)

3. (Currently Amended) An image sensor comprising an array of columns and rows of pixels (X_{ij}), all the pixels of one column of the array being connected to at least one common pixel output line (1_j) having at least one memory element (M_j) and at least one column amplifying element (A_j), all said column~~these~~ amplifying elements (A_j) being connected to a common output amplifier (D), ~~characterised in that before the amplifying element (A_j), the~~each common pixel output line (1_j) being~~is~~ divided through switches ($S4_j$ and $S5_j$) into~~in~~ at least two parallel circuits before the respective column amplifying element (A_j), at least one of these parallel circuits~~circuit~~ having said memory element (M_j), the two parallel circuits being connected through a switch ($S6_j$) with the same input of said column amplifying element (A_j), wherein there is a further switch (X_j) between said column amplifying element (A_j) and the common output amplifier (D) and wherein the image sensor is a CMOS or MOS device.

4. (Original) An image sensor as recited in claim 3, wherein both circuits have a memory element (Ms_j and Mr_j).

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (New) An image sensor as recited in claim 3, wherein said column amplifying elements (A_j) and the common output amplifier (D) are connected by a bus.

11. (New) An image sensor according to claim 3, wherein the image sensor has at least two input terminals.